



PATENT ABSTRACTS OF JAPAN

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H01L 21/76**H01L 21/316****H01L 21/762****H01L 27/12**(21) Application number: **2000286328**(71) Applicant: **NEC CORP**(22) Date of filing: **21.09.00**(72) Inventor: **KOBAYASHI KIYONARI**(54) **FORMING METHOD OF ISOLATION TRENCH**

(57) Abstract:

PROBLEM TO BE SOLVED: To provide a trench forming method by which the inside of the trench is possible to be filled so that it may not generate voids, and at the same time by which it is possible to flatten a concavity formed on the trench when forming the isolation trench of a semiconductor integrated circuit.

SOLUTION: The trench 5 extending to a buried insulating layer 3 is formed at a fixed place in a semiconductor layer 1 of a SOI substrate 10 having a buried insulation film 3. Thereafter, the trench 5 is completely buried with the NSG film 6 by forming the NSG film 6 on the whole surface, and a BPSG film 7 is grown on the NSG film 6. The surfaces of the BPSG film 7 and the NSG film 6 are made flat by etching back to a fixed thickness, after the surface of the BPSG film 7 is flattened by a thermal treatment. The NSG has a large surface migration and a good surface covering property, therefore, inside of the trench 5 can be filled so that no void is generated. The BPSG has a fluidity by a heat treatment so that the concavity formed on the surface of the NSG film on the trench 5 can be flattened. Therefore, according to this invention, it becomes possible to fill

the isolation trench with oxides, and to finish the surface flat.

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